REMARKS

The Office Action dated November 23, 2004 in this Application has been carefully considered. Claims 1-17 are pending. The above amendments and the following remarks are presented in a sincere attempt to place this Application in condition for allowance. Claims 1 and 11 have been amended in this Response. Claim 17 has been added in this Response. Reconsideration and allowance are respectfully requested in light of the above amendments and following remarks.

An interview was held with the Examiner, Mr. Tse Chen, on December 21, 2004 to discuss the rejections under 35 U.S.C. §§ 102(e) and 103(a) and the proposed amendments thereto. Applicant thanks the Examiner for the courtesies extended.

Claims 1-3, 8, and 11-13 stand rejected under 35 U.S.C. §102(e) in view of U.S. Patent No. 6,611,920 to Fletcher ("Fletcher"). Insofar as they may be applied against the Claims, these rejections are overcome.

Rejected independent Claim 1 as now amended more particularly recites one of the distinguishing characteristics of the present invention, namely, "control logic that is at least configured to generate at least one instruction-valid control bit, wherein the at least one instruction-valid control bit is configured to disable a first clock derived from the main processor clock if a first stage is unused or to disable a second clock derived from the main processor clock if a second stage is unused." Support for this Amendment can be found, among other places, page 6, lines 10-15 of the original Application.

Fletcher does not suggest, teach, or disclose generation of an instruction-valid bit. Specifically, Fletcher teaches a conventional pipeline such that when data is latched a valid bit is simultaneously propagated through the clock generation logic to provide a clocking signal at each successive stage. The present invention of Claim 1 does not simply utilize a pipeline to propagate a

valid bit. Instead, an instruction-valid bit is generated each time. This allows the present invention of Claim 1 to have increase flexibility so that data propagation can be terminated at any time as well as allowing a clocking signal to be provided at each stage, which Fletcher does not provide.

In view of the foregoing, it is apparent that the cited reference does not disclose, teach or suggest the unique combination now recited in amended Claim 1. Applicants therefore submit that amended Claim 1 is clearly and precisely distinguishable over the cited reference in a patentable sense, and is therefore allowable over this reference and the remaining references of record. Accordingly, Applicants respectfully request that the rejection of Claim 1 under 35 U.S.C. § 102(e) in view of Fletcher be withdrawn and that Claim 1 be allowed.

Claims 2, 3, and 8 depend on and further limit Claim 1. Hence, for at least the aforementioned reasons, these Claims would be deemed to be in condition for allowance. Applicants respectfully request that the rejections of dependent Claims 2, 3, and 8 also be withdrawn.

Applicants contend that the rejection of Claim 11 is overcome for at least some of the reasons that the rejection of Claim 1 as amended is overcome. These reasons include Fletcher not disclosing, teaching, or suggesting "*detecting when valid instructions are not being executed by one or more stages by control logic;* and reducing power consumption in the microprocessor by dynamically controlling the first and second clocks "*by disabling at least one local clock buffer to prevent switching of the first clock or the second clock.*" (Emphasis added.)

In view of the foregoing, it is apparent that the cited reference does not disclose, teach or suggest the unique combination now recited in amended Claim 11. Applicants therefore submit that amended Claim 11 is clearly and precisely distinguishable over the cited reference in a patentable sense, and is therefore allowable over this reference and the remaining references of record.

Accordingly, Applicants respectfully request that the rejection of Claim 11 under 35 U.S.C. § 102(e) in view of Fletcher be withdrawn and that Claim 11 be allowed.

Claims 12 and 13 depend on and further limit Claim 11. Hence, for at least the aforementioned reasons, these Claims would be deemed to be in condition for allowance. Applicants respectfully request that the rejections of dependent Claims 12 and 13 also be withdrawn.

Claims 4-7, 9, and 14-16 stand rejected under 35 U.S.C. §103(a) in view of Fletcher and U.S. Patent No. 6,304,125 by Sutherland ("Sutherland"). Insofar as they may be applied against the Claims, these rejections are overcome.

Claims 4-7 and 9 depend on and further limit Claim 1. As pointed out above, Fletcher does not suggest, teach, or disclose generation of an instruction-valid bit. Specifically, Fletcher teaches a conventional pipeline such that when data is latched a valid bit is simultaneously propagated through the clock generation logic to provide a clocking signal at each successive stage. The present invention of Claim 1 does not simply utilize a pipeline to propagate a valid bit. Instead, an instruction-valid bit is generated each time. This allows the present invention of Claim 1 to have increase flexibility so that data propagation can be terminated at any time as well as allowing a clocking signal to be provided at each stage, which Fletcher does not provide. Sutherland fails to cure this deficiency in Fletcher and, thus, even if hypothetically combined with Fletcher, would neither yield nor suggest the invention defined by Claims 4-7 and 9. Hence, for at least the aforementioned reasons, these Claims would be deemed to be in condition for allowance. Applicants respectfully request that the rejections of dependent Claims 4-7 and 9 also be withdrawn.

Claims 14-16 depend on and further limit Claim 11. Hence, for at least the aforementioned reasons, these Claims would be deemed to be in condition for allowance. Applicants respectfully request that the rejections of dependent Claims 14-16 also be withdrawn.

Claim 10 stands rejected under 35 U.S.C. §103(a) in view of Fletcher and U.S. Patent No. 6,629,250 by Kosper et al. ("Kosper"). Insofar as it may be applied against the Claim, this rejection is overcome.

Claim 10 depends on and further limits Claim 1. As pointed out above, Fletcher does not suggest, teach, or disclose generation of an instruction-valid bit. Specifically, Fletcher teaches a conventional pipeline such that when data is latched a valid bit is simultaneously propagated through the clock generation logic to provide a clocking signal at each successive stage. The present invention of Claim 1 does not simply utilize a pipeline to propagate a valid bit. Instead, an instruction-valid bit is generated each time. This allows the present invention of Claim 1 to have increase flexibility so that data propagation can be terminated at any time as well as allowing a clocking signal to be provided at each stage, which Fletcher does not provide. Kosper fails to cure this deficiency in Fletcher and, thus, even if hypothetically combined with Fletcher, would neither yield nor suggest the invention defined by Claim 10. Hence, for at least the aforementioned reasons, this Claim would be deemed to be in condition for allowance. Applicants respectfully request that the rejection of dependent Claim 10 also be withdrawn.

Applicants have now made an earnest attempt to place this Application in condition for allowance. For the foregoing reasons and for other reasons clearly apparent, Applicant respectfully requests full allowance of Claims 1-17.

Applicants do not believe that any fees are due; however, in the event that any fees are due, the Commissioner is hereby authorized to charge any required fees due (other than issue fees), and to credit any overpayment made, in connection with the filing of this paper to Deposit Account No. 50-0605 of CARR LLP.

Should the Examiner require any further clarification to place this application in condition for allowance, the Examiner is invited to telephone the undersigned at the number listed below.

Respectfully submitted,

CARR LLP

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